**IN THE CLAIMS:**

1. (Cancelled)

2. (Previously Presented) The shift register as defined in claim [[1]] 29, wherein M(M ≥ 2)kinds of clock signals are successively inputted to every [[(M - 1)]] M number of the flip-flops on a plurality of stages.

3. (Original) The shift register as defined in claim 2, wherein the M kinds of clock signals are allowed to have such phases that their high-level periods or low-level periods do not overlap each other.

4. (Original) The shift register as defined in claim 3, wherein the duty ratio of each of the M kinds of clock signals is preferably set to not more than (100 ×1/M)%.

5. (Cancelled).

6. (Cancelled).

7. (Previously Presented) The shift register as defined in claim [[1]] 29, further comprising:

an input stabilizing section for stabilizing an input to each of the flip-flops on the plural stages which the switching means is opened.

8. (Cancelled).

9. (Cancelled).

10. (Currently Amended) An image display device comprising:

a display section constituted by a plurality of pixels arranged in a matrix format;

a data signal line driving circuit, connected to a plurality of data signal lines, for supplying to the respective data signal lines image data to be written in the pixels; and

a scanning signal line driving circuit, connected to a plurality of scanning signal lines, for supplying to the scanning signal lines a scanning signal for controlling a writing operation of the image data to the pixels,

wherein the shift register as defined in claim [[1]] 29 is installed at least in either the data signal line driving circuit or the scanning signal line driving circuit.

11. (Original) The image display device as defined in claim 10, wherein at least either the data signal line driving circuit or the scanning signal line driving circuit is formed on a substrate on which the pixels are formed.

12. (Original) The image display device as defined in claim 10, wherein a switching element constituting at least either the data signal line driving circuit

or the scanning signal line driving circuit is a polycrystal silicon thin-film transistor.

13. (Original) The image display device as defined in claim 12, wherein the switching element is formed at a temperature of not more than 600 °C.

14. (Cancelled).

15. (Original) The shift register as defined in claim [[14]] 34, wherein each of the level shifter is provided with a current-driving type voltage-raising section.

16. (Cancelled).

17. (Cancelled).

18. (Original) The shift register as defined in claim [[14]] 34, wherein the level shifter comprises an output stabilizing means for maintaining an output voltage at a predetermined value at the time of stoppage.

19. (Cancelled).

20. (Original) The shift register as defined in claim [[14]] 34, wherein, supposing that M is an integer not less than 2, M kinds of clock signals are

successively inputted to every M number of the flip-flops on a plurality of stages.

21. (Original) The shift register as defined in claim 20, wherein each of the M kinds of clock signals is allowed to have either a phase in which high-level periods do not overlap each other or a phase in which low-level periods do not overlap each other.

22. (Original) The shift register as defined in claim 20, wherein the duty ratio of each of the M kinds of clock signals is set to not more than (100 ×1/M)%.

23. (Cancelled).

24. (Cancelled).

25. (Currently Amended) An image display device comprising:

a display section which includes a plurality of pixels arranged in a matrix format, a plurality of data signal lines placed on the respective columns of the pixels and a plurality of scanning signal lines placed on the respective rows of the pixels and which displays an image on the pixel by a data signal that is sent from the data signal line to each pixel in synchronism with a scanning signal supplied from each scanning signal line so as to form an image;

a scanning signal driving circuit for successively supplying scanning signals having different timing from each other to the scanning signal lines in synchronism with a first clock having a predetermined cycle; and

a data signal line driving circuit for extracting data signals applied onto the respective pixels on the scanning signal line to which the scanning signal has been applied, from a video image signal that has been successively applied in synchronism with a second clock having a predetermined cycle and is representative of a display state of each pixel, and for outputting the resulting data to each of the data signal lines,

wherein at least either the data signal line driving circuit and the scanning signal line driving circuit includes the shift register having the first or second clock signal as a clock signal as defined in claim [[14]] 34.

26. (Original) The image display device as defined in claim 25, wherein at least either the data signal line driving circuit or the scanning signal line driving circuit is formed on a substrate on which the pixels are formed.

27. (Original) The image display device as defined in claim 25, wherein the data signal line driving circuit, the scanning signal line driving circuit and the respective pixels include switching elements made of polycrystal silicon thin-film transistors.

28. (Original) The image display device as defined in claim 27, wherein the data signal line driving circuit, the scanning signal line driving circuit and

the respective pixels include switching elements that are formed at a temperature of not more than 600 °C.

29. (Previously Presented) A shift register comprising:

flip-flops of a plurality of stages; and

switching means of a plurality of stages, and

wherein:

the switching means on each of the stages is such that an input of a clock signal is controlled by the flip-flop on an immediately preceding stage controlling an open/closed state of that switching means through an output signal from that flip-flop; and

a clock signal inputted to the switching means which is ON is a set input to the flip-flop on an immediately succeeding stage and an output pulse from that succeeding stage in the shift register.

30. (Previously Presented) The shift register as defined in claim 2, wherein the flip-flop on each of the stages is a set-reset-type flip-flop, and an output pulse of the switching means controlled by the flip-flop on each one of the stages is inputted to a reset terminal of a flip-flop on a stage which precedes that stage by (kxM - 1) stages ($k \geq 1$).

31. (Previously Presented) The shift register as defined in claim 2, wherein: the flip-flop on each of the stages is a set-reset-type flip-flop; and an output signal of a flip-flop on each one of the stages is inputted to a reset

terminal of a flip-flop on a stage which precedes that stage by (kxM) stages (k $\geq$1).

32. (Previously Presented) The shift register as defined in claim 7, wherein the flip-flop on each of the stages is a set-reset-type flip-flop, and an output pulse of the switching means controlled by the flip-flop on each one of the stages is inputted to a reset terminal of a flip-flop on a stage which precedes that stage by (kxM - 1) stages (k $\geq$1).

33. (Previously Presented) The shift register as defined in claim 7, wherein: the flip-flop on each of the stages is a set-reset-type flip-flop; and an output signal of a flip-flop on each one of the stages is inputted to a reset terminal of a flip-flop on a stage which precedes that stage by (kxM) stages (k $\geq$1).

34. (Previously Presented) A shift register comprising:

flip-flops of a plurality of stages; and

level shifters of a plurality of stages, each for voltage-raising a clock signal,

wherein:

each of the level shifters is such that a clock signal voltage raising operation thereof is controlled by the flip-flop on an immediately preceding stage to that level shifter through an output signal from that flip-flop; and

the clock signal voltage-raised by that level shifter is an input to the flip-flop on an immediately succeeding stage and an output pulse from that succeeding stage in the shift register.

35. (Currently Amended) The shift register as defined in claim 15, wherein the output signal of the flip-flop on each one of the stages is inputted to the voltage-raising section of the level shifter on an immediately succeeding stage so that the corresponding level shifter is stopped by applying a signal having a level so as to cut off [[the]] an input switching element.

36. (Previously Presented) The shift register as defined in claim 15, wherein the output signal of the flip-flop on each one of the stages stops a power supply to the level shifter on an immediately succeeding stage so that the corresponding level shifter is stopped.

37. (Previously Presented) The shift register as defined in claim 34, wherein a transistor, which is installed in the level shifter on each one of the stages and to which a clock signal is inputted, has a gate capacitance that is separated from a transmission line of the clock signal by the output signal of the flip-flop on the immediately preceding stage.

38. (Previously Presented) The shift register as defined in claim 20, wherein the flip-flop on each of the stages is a set-reset-type flip-flop, and an output pulse of the switching means controlled by the flip-flop on each one of

the stages is inputted to a reset terminal of a flip-flop on a stage which precedes that stage by (kxM - 1) stages (k $\geq$1).

39. (Previously Presented) The shift register as defined in claim 20, wherein: the flip-flop on each of the stages is a set-reset-type flip-flop; and an output signal of a flip-flop on each one of the stages is inputted to a reset terminal of a flip-flop on a stage which precedes that stage by (kxM) stages (k $\geq$1).